Remarks

In the Office Action dated January 29, 2010 the Examiner maintained the restriction/election requirement, withdrawing claims 8, 10, 11, 13 and 15-16 from consideration. The following rejections are presented: claims 1, 3, 5 and 7 stand rejected under 35 U.S.C. § 103(a) over Chang (U.S. Patent No. 5,991,204) in view of Sharma (U.S. Patent 5,488,579) and further in view of a Quirk reference ("Semiconductor Manufacturing Technology"); claims 4 and 14 stand rejected under 35 U.S.C. § 103(a) over the '204, '579 and Quirk references and further in view of Hong (U.S. Patent No. 5,614,746); and claim 6 stands rejected under 35 U.S.C. § 103(a) over the '204, '579 and Quirk references and further in view of Chen (U.S. Patent No. 6,091,104). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Advisory Action dated June 10, 2009, or the Office Actions of record.

Applicant notes that various rejections appear to be repeated word-for-word, and further that the Response to Arguments section fails to address many of Applicant's traversals. Applicant therefore fully incorporates its traversals of record herein, and requests that the Examiner fully addresses these traversals and those as presented below.

Applicant maintains its traversals regarding the restriction requirement for reasons as stated in the record, as the rationale provided in support of the restriction is misguided and fails to comply with the requirements of the M.P.E.P., that the Examiner establish that a serious burden. Specifically, M.P.E.P. § 803 indicates that establishing a *prima facie* serious burden can be shown "by appropriate explanation of separate classification, or separate status in the art, or a different field of search as defined in MPEP § 808.02." In this instance, the instant Office Action fails to establish such *prima facie* burden in attempting to support the restriction by asserting that "there were a lot of amendments." Moreover, the amendments in various restricted claims (in response to which the restriction requirement was issued) were relatively minor. As an example, independent claim 8 was amended to change the limitation "a floating gate dielectric" to "a dielectric layer" to maintain consistent terminology. Independent claim 11 was similarly amended. The Examiner's assertion that examining these (and similar) claims as amended would present "undue burden" fails to meet the *prima facie* requirements as discussed in the

M.P.E.P. Applicant therefore submits that the restriction is improper, and further believes that the claims should be allowable over the cited references for reasons including those stated in the record and herein.

The § 103(a) rejections are improper because the Office Action's failure to address and afford weight to all claim limitations is based upon allegations regarding apparatus/device-based limitations, yet the claims at issue are method claims. Referring to page 10 of the Office Action, the Examiner's assertion that "an element [that] is adapted to perform a function is not a positive limitation" is inapplicable to method-based limitations including those directed to "using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer." Furthermore, the Examiner's reliance upon In re Hutchinson regarding these "adapted to" assertions apply to claims using these terms, whereas these terms are not present in any of the instant claims. Moreover, the secondary '579 reference cannot mitigate oxygen diffusion as suggested because the dielectric arrangement as part of an inverted gate structure does not permit the spacers to do so as discussed further below. Accordingly, the Examiner has failed to establish correspondence to relevant limitations in independent claim 1, rendering all rejections improper.

The § 103(a) rejections are further improper because the cited combination of references lacks correspondence. For example, none of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding forming a control gate and a floating gate separated by an interlayer dielectric layer, with spacers that are both arranged and used to mitigate oxygen diffusion to the interlayer dielectric layer. Because none of the references teach these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejections fail.

The cited spacers in the secondary '579 reference do not and cannot mitigate oxygen diffusion as suggested because their arrangement as part of an inverted gate structure does not permit the spacers to do so. Combining the inverted-gate manufacturing approach of the '579 reference with the (conventional) gate stack of the flash EEPROM device in the primary '204 reference does not result in the claimed method as suggested in the Office Action. Essentially, the Examiner's rejection relies upon an assertion that the cited spacers *could* mitigate oxygen diffusion to an interlayer

dielectric material if arranged and used as such; however, nothing in the record establishes that the purported combination of an inverted-gate structure with the gate stack in the '204 reference would correspond, and nothing in the record suggests doing so in order to mitigate diffusion (in the context of the method-based limitations or otherwise).

More specifically, the Examiner's assertion that the secondary '579 reference teaches using spacers to mitigate the diffusion of oxygen to a deposited interlayer dielectric layer, "[b]ecause the oxygen has to diffuse across the spacer before reaching the interlayer dielectric layer" is erroneous. The cited spacers in the inverted gate structure of the '579 reference cannot and do not mitigate oxygen diffusion as claimed because they are not positioned to do so. The inverted gate structure in the '579 reference is further unrelated to the (conventional) structure of the '204 reference and issues relating to the manufacture of the same. Due to this inverted structure, gate oxides 35 and 38 of the '579 reference are completely exposed during any subsequent oxide growth, relative to the spacers 37. The cited spacers 37 therefore do not mitigate the diffusion of oxygen in an interlayer dielectric layer because such layers are formed over the spacer (*e.g.*, tunnel oxide 38 is formed over and after the spacer 37, which thus cannot mitigate any diffusion as asserted). The Office Action is further silent as to how to combine the inverted-gate manufacturing approach of the '579 reference with the manufacture of a conventional gate stack for the EEPROM device in the '204 reference. Accordingly, none of the cited references teach or suggest limitations directed to using spacers to both mask an underlying gate and mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

The §103(a) rejections are further improper because there is no motivation to combine the cited inverted-gate manufacturing approach of the '579 reference with the gate stack manufacturing steps of the '204 reference. Specifically, the Examiner has failed to provide any explanation as to how the inverted-gate manufacturing approach in the '579 reference, which uses a nitride spacer 37 to "smooth the topography created by the polysilicon gate 36" and to address specific problems with inverted-gate structures as in FIG. 3, would apply to the conventional gate stack of the EEPROM device in the '204 reference. Nothing in the asserted art either explains how this inverted-gate approach

would either be applicable to or combined with the EEPROM gate stack in the '204 reference. Moreover, Applicant fails to recognize how this combination of teachings would result in an implementation that is operable and consistent with the objectives of the '204 reference. As consistent with the M.P.E.P. and relevant case law, if a "proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *See* M.P.E.P. 2143.01, citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984). This attempt at modifying the '204 reference without providing examples from the prior art in support of such modification is further contrary to § 103 and relevant law (*see KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007), requiring evidence of motivation where the primary reference is modified).

The Office Action has also failed to establish motivation to combine the dry etch of the Quirk reference with the '204 reference, as consistent with Applicant's traversals of record, contrary to the requirements of the M.P.E.P. and applicable law (*see*, *e.g.*, the *KSR* reference as cited above). In this instance, the alleged motivation to combine the Quirk reference with the '204 reference is to provide "high selectivity and low device damage" but is silent as to how these features would be applicable to the conventional gate structure of the '204 reference or how the '204 reference could function as such. For example, while the Office Action provides no discussion as to how the dry etch in the Quirk reference would be combined with the '204 reference as modified with the inverted-gate approach as shown in the '579 reference, it appears such a dry etch would be inapplicable as there are no underlying dielectric regions due to the inverted nature of the structure.

Applicant has added new claims 17-19. Applicant believes these claims to be allowable over the cited references for reasons including those stated above, and because the cited combination of references appears to fail to disclose, teach or suggest limitations including those directed to forming a spacer between a control gate and an access gate, and to forming a floating gate sidewall dielectric that is contiguous with an access gate dielectric and located between a floating gate and an access gate. Applicant notes that support for claims 17-19 can be found throughout Applicant's disclosure, with exemplary

embodiments described, for example, in Figure 10 and the discussion relating to Figure 10 in Applicant's specification.

In view of the above, the § 103 rejections are improper and Applicant requests that they be withdrawn. Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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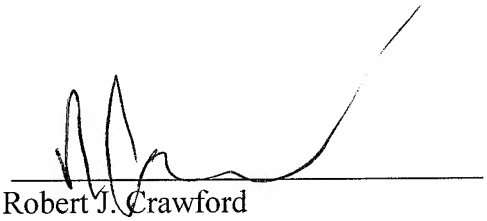
By: 

Robert J. Crawford
Reg. No.: 32,122
Eric J. Curtin
Reg. No.: 47,511
(NXPS.442PA)